A Simple Technique for Minimization of ABC-Induced Error in the FDTD Analysis of Microstrip Discontinuities

Xing Ping Lin and Krishna Naishadham, *Member, IEEE*

Abstract—**Imperfectly absorbing truncation boundaries in the simulation of microstrip circuits by the finite-difference time-domain (FDTD) method necessitate large computational domains, imposing a significant burden on the resources. Residual boundary reflection sometimes causes serious degradation of the computed parameters (e.g., oscillatory behavior). We introduce a simple modification of the FDTD implementation for microstrip discontinuities, wherein two sub-problems whose domains are reduced by bringing the absorbing boundary close to the circuit, are superposed to cancel the dominant boundary reflection. Computed results on transmission line and resonant type discontinuities demonstrate that significant computational savings can be achieved without compromising accuracy.**

I. Introduction

The finite-difference time-domain (FDTD) method has been used by many researchers to characterize planar transmission lines and microstrip circuit elements (see [1]–[3]). In order to truncate the computational domain and simulate the radiation boundary condition required of outgoing waves relevant to open structures, various absorbing boundary conditions (ABC) have been introduced [4]. Since none of them result in fully transparent boundaries, they will introduce some error in the computed frequency-domain circuit parameters. In order to minimize this error, the absorbing walls are usually placed sufficiently far away from the components, thereby requiring considerable computational resources.

In this letter, we describe a simple procedure in which two sub-problems, differing in geometry only in the position of the absorbing wall, are superposed such that dominant reflection from the absorbing boundary is canceled in the combined solution. For further references, we term the procedure as the geometry rearrangement technique (GRT). Although we have chosen Mur's first-order ABC in the FDTD implementation, GRT can correct the error introduced by any ABC used. Computed results on microstrip discontinuities indicate that the longitudinal absorbing boundary can be located just one cell beyond the appropriate reference plane, and yet accurate results can be obtained in comparison with conventional FDTD implementation. Since much smaller computational domain is used in GRT, the results also demonstrate significant savings in resources.

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The authors are with the Department of Electrical Engineering, Wright State University, Dayton, OH 45435 USA.

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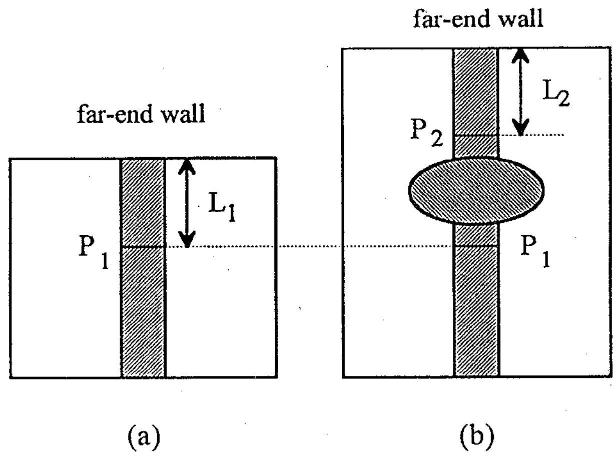

Fig. 1. (a) Transmission line. (b) Two-port discontinuity.

II. GRT Implementation

Two auxiliary problems with different absorbing boundary locations (see Fig. 1) are superposed to cancel the dominant ABC-induced reflection in the calculation of S-parameters of microstrip discontinuities. With P_1 and P_2 denoting input and output reference plane locations, the transmission parameter is given by [3]

$$S_{21} = \frac{V_2}{V_1} \tag{1}$$

where V_1 and V_2 are voltages calculated in the frequency domain by Fourier transformation of the corresponding time-domain signals. The transmission line (Fig. 1(a)) is simulated to obtain the incident voltage V_1 in the plane P_1.

In conventional FDTD implementation, the transmission lines connected to the ports are chosen long enough such that the incoming and outgoing waves at each port are least affected by reflection from the absorbing boundary (see [3]). In the absence of any such reflection, (1) yields the correct S_{21}. We will now examine how the inevitable boundary reflection influences (1). Let the transmission lines in Fig. 1(a) and 1(b) be identical, and let Γ, β be the **frequency-dependent** reflection coefficient at the far-end wall and phase constant, respectively, of the dominant propagating mode. Then, the

TABLE I
MEMORY AND CPU REQUIREMENTS ON A CRAY YMP SUPERCOMPUTER

Circuit	T-Junction				Low-Pass Filter		
Method	Conventional FDTD	GRT (1)	GRT (2)	GRT (3)	Conventional FDTD	GRT (1)	GRT (2)
$L_2/\Delta y$	29	29	4	1	34	5	1
$L_1/\Delta y$	64	29	4	1	54	5	1
Memory (megawords) Comparison	1.68+1.42=3.1 100%	1.22+1.42=2.64 85%	0.90+1.10=2.0 64.5%	0.86+1.06=1.92 61.9%	0.99+1.18=2.17 100%	0.76+0.55=1.31 60.4%	0.72+0.50=1.22 56.2%
CPU time (s) Comparison	1360+284=644 100%	220+284=504 78%	164+196=360 56%	156+184=340 52.7%	905+730=1,635 100%	650+285=935 57.2%	613+260=873 53.4%

discontinuity parameter is calculated from transmission line theory as

$$S_{21} = \frac{V_2}{V_1}\frac{1+\Gamma e^{-j2\beta L_2}}{1+\Gamma e^{-j2\beta L_1}} \quad (2)$$

where L_1 and L_2 are defined in Fig. 1 and the reference planes P_1 and P_2 are located sufficiently far away (usually 5 to 10 cell lengths) from the discontinuity such that the higher-order modes have decayed substantially. Likewise, the source-end boundary is far enough such that its reflection can be neglected in comparison with the (dominant) reflection from the far-end boundary. In GRT, we choose $L_1 = L_2$ (Fig. 1), so that the ratio of the two sampled voltages in (2) becomes independent of the reflection coefficient, Γ, and makes (2) **identical** with (1). Thus, the far-end boundary reflection is indeed **canceled**, thereby allowing for positioning of this boundary very close to the reference port in either sub-problem and permitting significant computational savings. The influence of boundary reflection on S_{11} cannot be canceled as described above. Instead, it is possible to correct S_{11} by estimating the reflection coefficient, as explained in [5]. We have numerically found that the absorbing boundary does not strongly excite the higher-order modes, so that accurate results for all the S-parameters can be obtained by terminating the computational domain longitudinally as close as 1 to 5 cells (in contrast to 30 or more in conventional method) behind the reference port.

III. NUMERICAL RESULTS AND EFFICIENCY

In order to demonstrate the computational efficiency of GRT, we choose a T-junction depicted in Fig. 2. The parameters used in the calculation are $\Delta x = \Delta y = 0.178$ mm, $\Delta z = 0.1588$ mm, $\Delta t = 0.24$ ps, $N_X = 85$, $N_Z = 25$, and the number of time steps, $N = 4{,}096$. Because of the relatively smooth discontinuity, we expect a strong detrimental influence of boundary reflection since the magnitude of S_{21} will be nearly unity and that of S_{11} will be nearly zero. GRT can reduce this influence considerably.

First, we use the conventional FDTD method to calculate S_{21}, choosing L_2 long enough to reduce the influence of far-end wall when calculating the output voltage V_2 and L_1 long enough to simulate the infinite transmission line when calculating the input voltage V_1. Then, we use the GRT-FDTD implementation with $L_1 = L_2$. Table I shows the computational savings of GRT over conventional FDTD, obtained by progressively decreasing L_1 or L_2, and thus moving the boundary closer to the circuit. The first term in the memory and CPU time listing pertains to the calculation

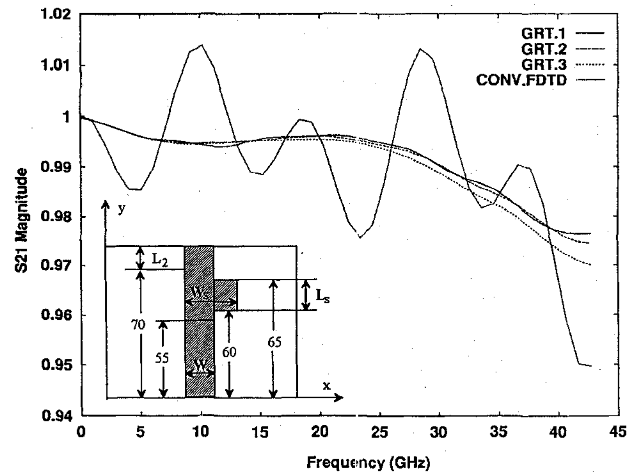

Fig. 2. Magnitude of S_{21} for the microstrip T-junction. $\epsilon_r = 2.2$, $h = 0.794$ mm, $W = 3.204$ mm, $W_S = 3.56$ mm, and $L_s = 0.89$ mm (see inset). Longitudinal dimensions are indicated by cell numbers. The distance from the reference plane of port 2 to the far-end boundary, L_2, is shown in Table I for the three GRT cases.

of V_1 and the second term to that of V_2. Fig. 2 displays as a function of frequency, the magnitude of S_{21} corresponding to the three GRT cases mentioned in Table I. The conventional FDTD result oscillates around the GRT result and is larger than unity over some frequency ranges (obviously incorrect) because of the large error introduced by reflection from the far-end boundary. GRT cancels this error, and hence, depicts a smooth result. The maximum difference in $|S_{21}|$ among the three GRT cases is found to be less then 0.4%. From Table I, the savings in computer memory and CPU time are found to be 38.1% and 47.3%, respectively, when the far-end boundary is located just one cell behind the output reference plane.

Fig. 3 shows GRT-computed insertion loss of a microstrip low-pass filter, simulated by the conventional FDTD method in [3]. The reference planes are chosen to be 10 cells away from the edges of the filtering stub, and the far-end boundary is located five cells away from the output reference plane. The other FDTD parameters are detailed in [3]. The GRT simulation is run for 4,096 and 8,192 time steps. The former misses the sharp resonance near 7 GHz. Therefore, 8,192 time steps are employed in the comparison of computational requirements of GRT and conventional FDTD, displayed in Table I. Also shown are these requirements with the boundary located just one cell behind the output plane. As seen in Fig. 3, the one- and five-cell results virtually overlap and compare very well with the measurements from [3] in predicting the sharp roll-off and the cut-off frequency of the filter.

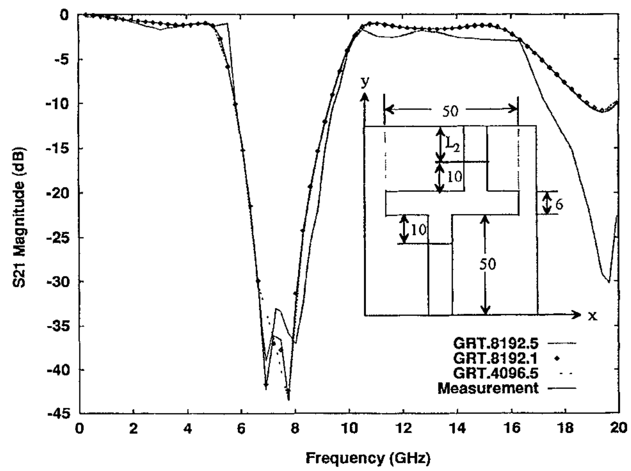

Fig. 3. Insertion loss of the microstrip low-pass filter with detail shown in [3], Fig. 7. Dimensions are indicated by cell numbers (inset). The first number besides GRT in the legend corresponds to the number of time steps and the second to $L_2/\Delta y$, indicated in Table I.

It is observed from Table I that about 45% savings are accomplished in both memory and CPU time with one-cell GRT vis-a-vis conventional FDTD.

IV. Conclusion

We have presented a simple technique to minimize ABC-induced error in the FDTD analysis of microstrip discontinuities. By moving the far-end absorbing wall only one cell behind the output reference plane for resonant as well as transmission line structures, we have shown that significant computational savings can be obtained over the conventional FDTD method without compromising accuracy of the computed results. It seems that the analysis presented in this paper can be extended to remaining absorbing walls by treating the computational domain as a cavity with weak penetration and employing standard waveguide theory to represent multiple reflections of either propagating or evanescent modes at these walls.

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